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| 1 | 4 | ((("6075932") or ("6151568") or ("6321185") or ("6363515")) .PN. | USPAT | 2004/10/13 18:43 |

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| 11 | 1742 | ((716/4) or (716/18) or (716/14)).CCLS. | USPAT | 2004/10/13 18:05 |
| 13 | 1 | (((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl and (high adj level adj language) same instruction | USPAT | 2004/10/13 18:06 |
| 14 | 1 | (((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl and ((high adj level adj language) same instruction) | USPAT | 2004/10/13 18:06 |
| 12 | 66 | (((716/4) or (716/18) or (716/14)).CCLS.) and (power same model) and rtl | USPAT | 2004/10/13 18:10 |
| 15 | 106 | (703/18).CCLS. | USPAT | 2004/10/13 18:10 |
| 16 | 5 | ((703/18).CCLS.) and (power same model) and rtl | USPAT | 2004/10/13 18:11 |

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|----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|------------------|
| 1 | 8881 | (hardware same software) and instruction\$2 and (simulator or simulation) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:29 |
| 2 | 1220 | ((hardware same software) and instruction\$2 and (simulator or simulation)) and dependency | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:29 |
| 3 | 519 | ((hardware same software) and instruction\$2 and (simulator or simulation)) and dependency and power and (usage or consumption) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:30 |
| 4 | 2 | ((hardware same software) and instruction\$2 and (simulator or simulation)) and dependency and power and (usage or consumption) and (capture\$2 same (gate-level or gate adj level)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:36 |
| 5 | 31 | refine same (data adj model) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:47 |
| 6 | 0 | refine same ((power or energy) near model) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:47 |
| 7 | 113 | refine same ((power or energy) and model) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:48 |
| 8 | 28 | (refine same ((power or energy) and model)) and SOC | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2004/10/13 13:50 |
| 9 | 40330 | model same (change or modification or refinement) | USPAT | 2004/10/13 13:50 |
| 10 | 1281 | model adj (change or modification or refinement) | USPAT | 2004/10/13 13:51 |
| 11 | 66 | (model adj (change or modification or refinement)) and (power adj consumption) | USPAT | 2004/10/13 14:30 |
| 12 | 9 | US-5481469-\$.DID. OR US-5870308-\$.DID. OR US-5572436-\$.DID. OR US-5801958-\$.DID. OR US-5696694-\$.DID. OR US-5682320-\$.DID. OR US-5838579-\$.DID. OR US-5838947-\$.DID. OR US-5903476-\$.DID. | USPAT | 2004/10/13 14:31 |
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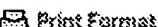
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Pages:856 - 863

[Abstract] [PDF Full-Text (455 KB)] IEEE JNL

2 Instruction-based system-level power evaluation of system-on-a-chip peripheral cores

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[Abstract] [PDF Full-Text (644 KB)] IEEE CNF

3 Trace-driven system-level power evaluation of system-on-a-chip peripheral cores

Givargis, T.D.; Vahid, F.; Henkel, J.;
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4 Evaluation of architecture-level power estimation for CMOS RISC processors

Sato, T.; Ootaguro, Y.; Nagamatsu, M.; Tago, H.;
Low Power Electronics, 1995., IEEE Symposium on , 9-11 Oct. 1995
Pages:44 - 45

[Abstract] [PDF Full-Text (172 KB)] IEEE CNF

5 A retargetable VLIW compiler framework for DSPs with instruction-level

parallelism

Rajagopalan, S.; Rajan, S.P.; Malik, S.; Rigo, S.; Araujo, G.; Takayama, K.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 , Issue: 11 , Nov. 2001
Pages:1319 - 1328

[Abstract] [PDF Full-Text (200 KB)] IEEE JNL

6 Power analysis of embedded software: a first step towards software power minimization

Tiwari, V.; Malik, S.; Wolfe, A.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 2 , Issue: 4 , Dec. 1994
Pages:437 - 445

[Abstract] [PDF Full-Text (912 KB)] IEEE JNL

7 SEA: fast power estimation for micro-architectures

Kalla, P.; Henkel, J.; Xiaobo Sharon Hu; ASIC, 2003. Proceedings. 5th International Conference on , Volume: 2 , 21-24 Oct. 2003
Pages:1200 Vol.2

[Abstract] [PDF Full-Text (316 KB)] IEEE CNF

8 Instruction level power analysis and optimization of software

Tiwari, V.; Malik, S.; Wolfe, A.; Lee, M.T.-C.; VLSI Design, 1996. Proceedings., Ninth International Conference on , 3-6 Jan. 1996
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[Abstract] [PDF Full-Text (368 KB)] IEEE CNF

9 Deterministic clock gating for microprocessor power reduction

Hai Li; Bhunia, S.; Chen, Y.; Vijaykumar, T.N.; Roy, K.; The Ninth International Symposium on High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. , 8-12 Feb. 2003
Pages:113 - 122

[Abstract] [PDF Full-Text (350 KB)] IEEE CNF

10 Exploiting reconfigurability for low-power control of embedded processors

Carro, L.; Correa, E.; Cardozo, R.; Moraes, F.; Bampi, S.; Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on , Volume: 5 , 25-28 May 2003
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11 Introducing pipelining technique in an object-oriented processor

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Cheng-Ta Hsieh; Lung-Sheng Chen; Pedram, M.;
Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001.
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14 Exploring optimal cost-performance designs for Raw microprocessors

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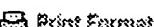
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MPEG-4. 2001 Proceedings of Workshop and Exhibition on , 18-20 June 2001

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